REMARKS

Claims 1-4, 6-20, 24-26, 29-30 and 33-37 are pending in this application. By this Amendment, claims 1, 4, 6, 9-11, 14, 18, 24, 29-30 and 33 are amended and claims 22-23, 27-28 and 31-32 are canceled without prejudice or disclaimer. Various amendments are made for clarity and are unrelated to issues of patentability.

The Office Action rejects claims 1-4, 6-20 and 22-37 under 35 U.S.C. §103(a) over U.S. Patent 5,365,475 to Matsumura et al. (hereafter Matsumura) in view of newly-cited U.S. Patent 4,901,285 to Sano et al. (hereafter Sano) and newly-cited U.S. Patent 6,593,799 to De et al. (hereafter De). The rejection is respectfully traversed with respect to the pending claims.

Independent claim 1 recites a first transistor pair and a second transistor pair coupled between the supply voltage line and GROUND, the supply voltage line to receive a first supply voltage based on an ACTIVE mode of the memory device and to receive a second supply voltage based on a STANDBY mode of the memory device, the second supply voltage being different than the first supply voltage. Independent claim 1 also recites a first access transistor, a second access transistor, and a bias transistor coupled to a body of one of the transistors of the first transistor pair and to a body of one of the transistors of the second transistor pair, the bias transistor to apply a forward body bias to the one transistor of the first transistor pair and to the one transistor of the second transistor pair based on the memory device being in the STANDBY mode.

The applied references do not teach or suggest at least these features of independent claim 1. More specifically, the applied references do not teach or suggest a

supply voltage line to receive a first supply voltage based on an ACTIVE mode of the memory device and to receive a second supply voltage based on a STANDBY mode of the memory device, the second supply voltage being different than the first supply voltage.

The Office Action asserts that Matsumura's SRAM mode/ACTIVE mode corresponds to a first mode and Matsumura's ROM mode (storing on data) corresponds to a second mode. However, Matsumura does not teach or suggest applying different supply voltages based on a mode of a memory device. Rather, Matsumura applies different supply voltages based on a type of cell (such as A type, B type, C type and D type cells). See, for example, col. 4, lines 11-13 and 53-58; col. 6, lines 55-68 and FIG. 8A. Matsumura's discussion of an SRAM and a ROM do not relate to modes (i.e., ACTIVE or STANDBY) of a memory device. Matsumura does not teach or suggest the supply voltage line to receive a first supply voltage based on an ACTIVE mode of the memory device and to receive a second supply voltage based on a STANDBY mode of the memory device.

The other applied references do not teach or suggest these features of independent claim 1 missing from Matsumura. The Office Action (on page 5) states that Matsumura does not disclose the STANDBY mode. The Office Action then relies on Sano's FIGs. 1A, 1B; col. 4, lines 11-13, 36-37 and lines 46-52 as allegedly teaching these features. However, the cited section merely relates to during operation of ROM 10 while not being read (standby mode). In this circumstance, ROM enable circuitry 62 puts ROM 10 in a pre-charge state. See, for example, col. 4, lines 36-48. The Office Action's assertions on pages 5-6 do not correspond to proper motivation to combine the references. Additionally, the Office Action's assertions on pages 5-6 do not make sense. Accordingly, the combination

based on Sano does not teach or suggest the features of independent claim 1 missing from Matsumura.

Further, the Office Action (on page 6) states that Matsumura and Sano do not teach or suggest a bias transistor to apply a forward body bias to the one transistor of the first transistor pair and to the one transistor of the second transistor pair based on STANDBY signal. Applicants submit that independent claim 1 is amended merely for clarity to recite based on the memory device being in the STANDBY mode. The Office Action then cites De's FIG. 7, col. 2, lines 2-6 and col. 6, lines 15-17 and 32-34 for the features of independent claim 1 missing from Matsumura and Sano. However, De very specifically discloses that a forward body bias is applied to transistors 340 and 342 in an active mode. See col. 6, lines 17- 21. De's active mode does not correspond to the claimed STANDBY mode. De also discloses operations in a standby mode. See col. 6, lines 25-29. However, this section does not suggest a forward body bias. Accordingly, the Office Action's assertions with respect to De are incorrect. De does not teach or suggest to supply a forward body bias based on a device being in a STANDBY mode.

Further, De does not teach or suggest applying a forward body bias when a memory device is in a STANDBY mode. That is, De does not relate to a memory device (as recited in independent claim 1 or in Matsumura). De relates to a NAND gate circuit 336 and how switches may apply body biases (such as via a voltage control circuitry 356). See De's col. 6, lines 12-15. Therefore, the Office Action's alleged combination with De is improper.

Applicants respectfully submit that Matsumura may not be combined by Sano and/or De so as to teach or suggest to apply a forward body bias based on the memory device

being in the STANDBY mode, as recited in independent claim 1. That is, De's description of a forward bias may not be combined with Matsumura/Sano to reach the features of independent claim 1.

For at least the reasons set forth above, Matsumura, Sano and De do not teach or suggest all the features of independent claim 1. For example, the applied references as a whole do not teach or suggest the bias transistor to apply a forward body bias to the one transistor of the first transistor pair and to the one transistor of the second transistor pair based on the memory device being in the STANDBY mode. Thus, independent claim 1 defines patentable subject matter

Independent claim 9 recites a first SRAM memory cell and a supply voltage line to provide a first supply voltage to two transistors of the at least four transistors of the first SRAM memory cell when the first SRAM memory cell is in an ACTIVE mode and to provide a second supply voltage to the two transistors when the first SRAM memory cell is in a STANDBY mode, the second supply voltage being different than the first supply voltage. Independent claim 9 also recites a switching device to apply a forward body bias to the two transistors of the cross-coupled inverter configuration of the first SRAM memory cell when the first SRAM memory cell is in the STANDBY mode.

For at least similar reasons as set forth above, the applied references do not teach or suggest at least these features of independent claim 9. The applied references do not teach or suggest to apply a forward body bias when the first SRAM memory cell is in the STANDBY mode. Thus, independent claim 9 defines patentable subject matter.

Independent claim 18 recites a static random access memory (SRAM) device and a power control unit to control a supply voltage level applied to the SRAM device and to provide a signal indicative of a mode of the SRAM device, the power control unit to apply a first voltage level when the SRAM device is in an ACTIVE mode and to apply a second voltage level when the SRAM device is in a STANDBY mode. Independent claim 18 also recites that the SRAM device includes a switching device to apply a forward bias to transistors within the SRAM device based on the signal provided by the power control unit indicative of the STANDBY mode of the SRAM device.

For at least similar reasons as set forth above, the applied references do not teach or suggest at least these features of independent claim 18. The applied references do not teach or suggest to apply a forward bias based on a signal provided by the power control unit indicative of the STANDBY mode of the SRAM device. Thus, independent claim 18 defines patentable subject matter.

For at least the reasons set forth above, each of independent claims 1, 9 and 18 define patentable subject matter. Each of the dependent claims depends from one of the independent claims and therefore defines patentable subject matter at least for this reason. In addition, the dependent claims recite features that further and independently distinguish over the applied references.

CONCLUSION

In view of the foregoing, it is respectfully submitted that the application is in condition for allowance. Favorable consideration and prompt allowance of claims 1-4, 6-20, 24-26, 29-30 and 33-37 are earnestly solicited. If the Examiner believes that any additional

changes would place the application in better condition for allowance, the Examiner is invited to contact the undersigned attorney at the telephone number listed below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this, concurrent and future replies, including extension of time fees, to Deposit Account 16-0607 and please credit any excess fees to such deposit account.

Respectfully submitted,
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